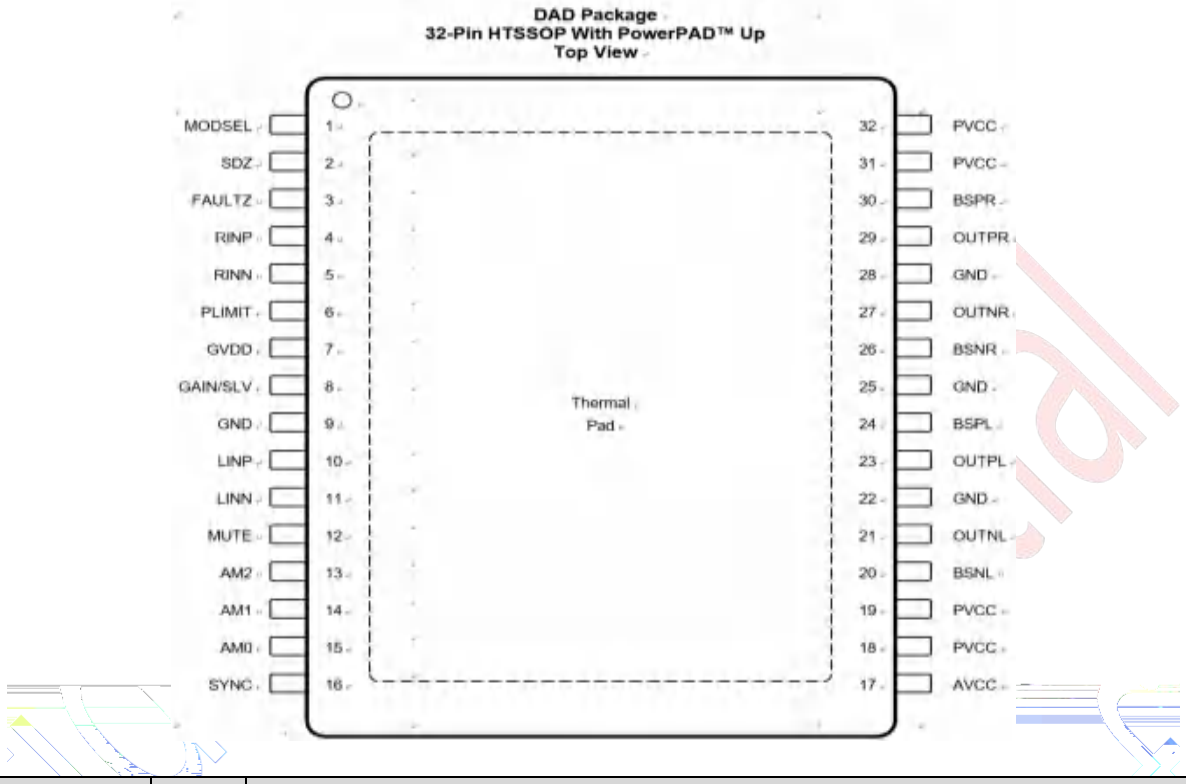
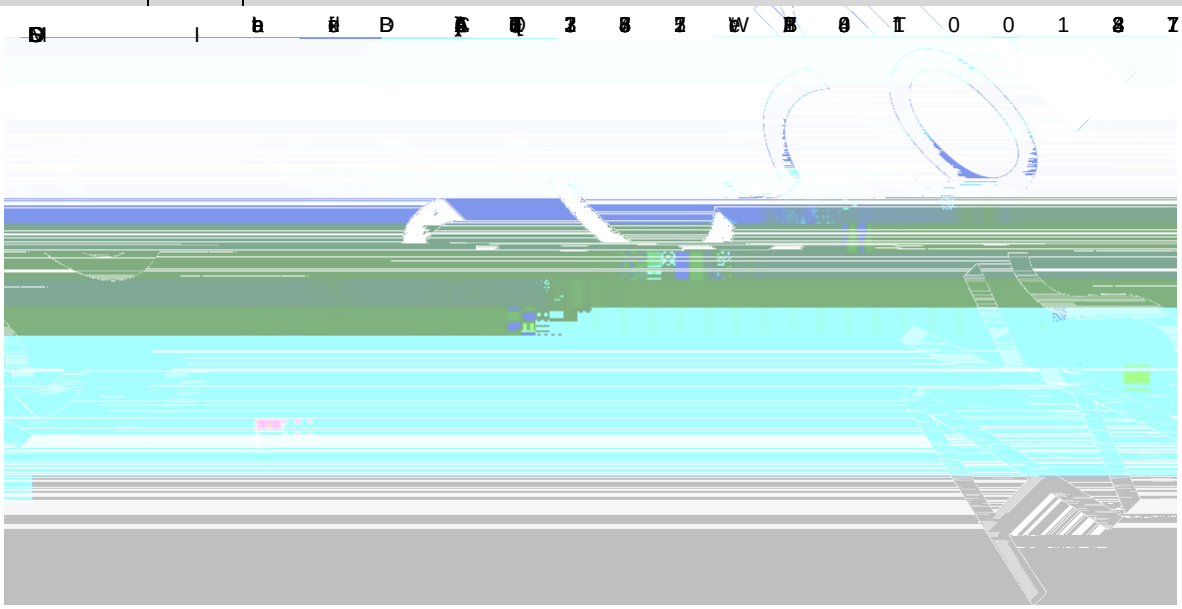
Description

Pin Configuration and Functions



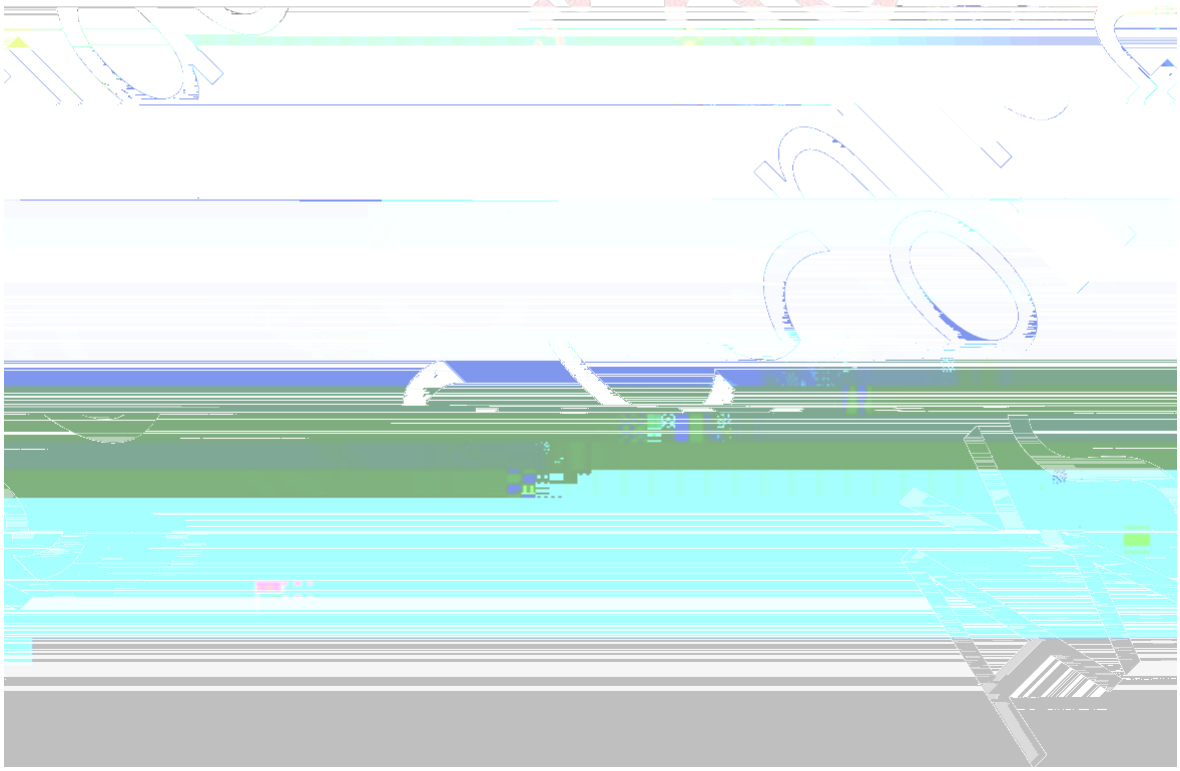
PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	[illegible]	[illegible]	[illegible] 0 0 1 [illegible]



3. Recommended Operating Conditions

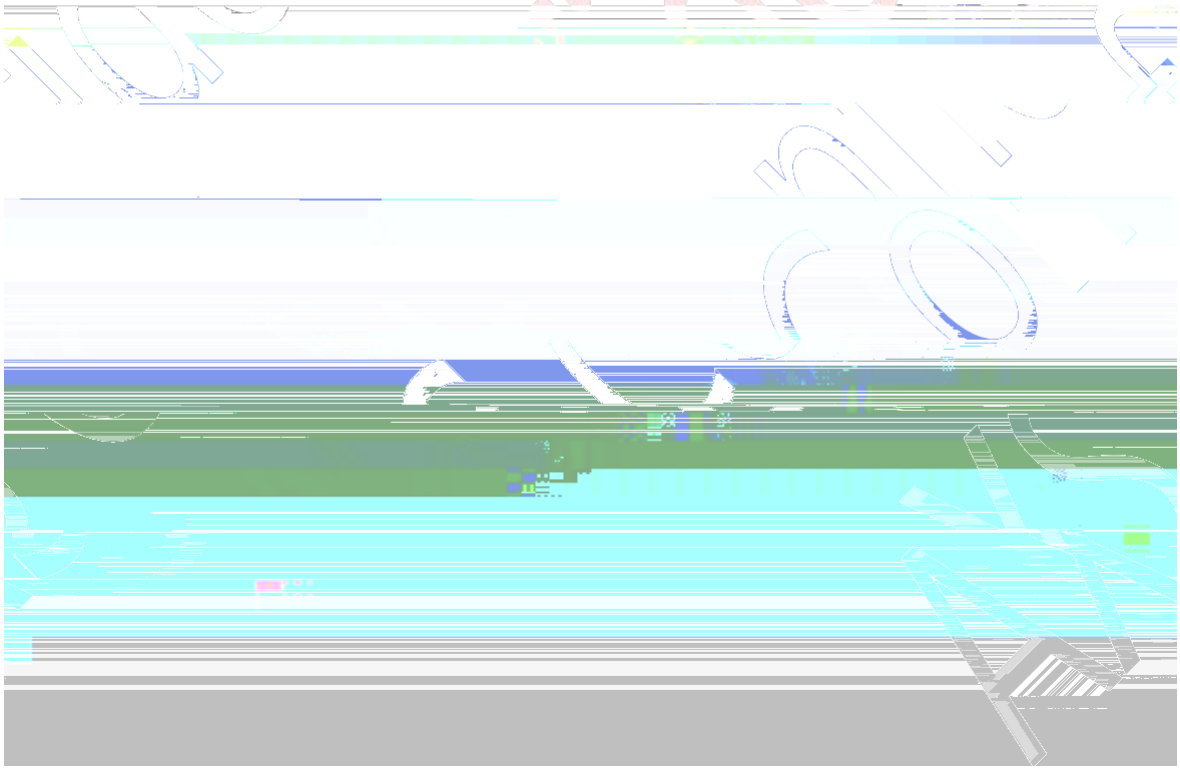
over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_C		5		12	V
V_H					



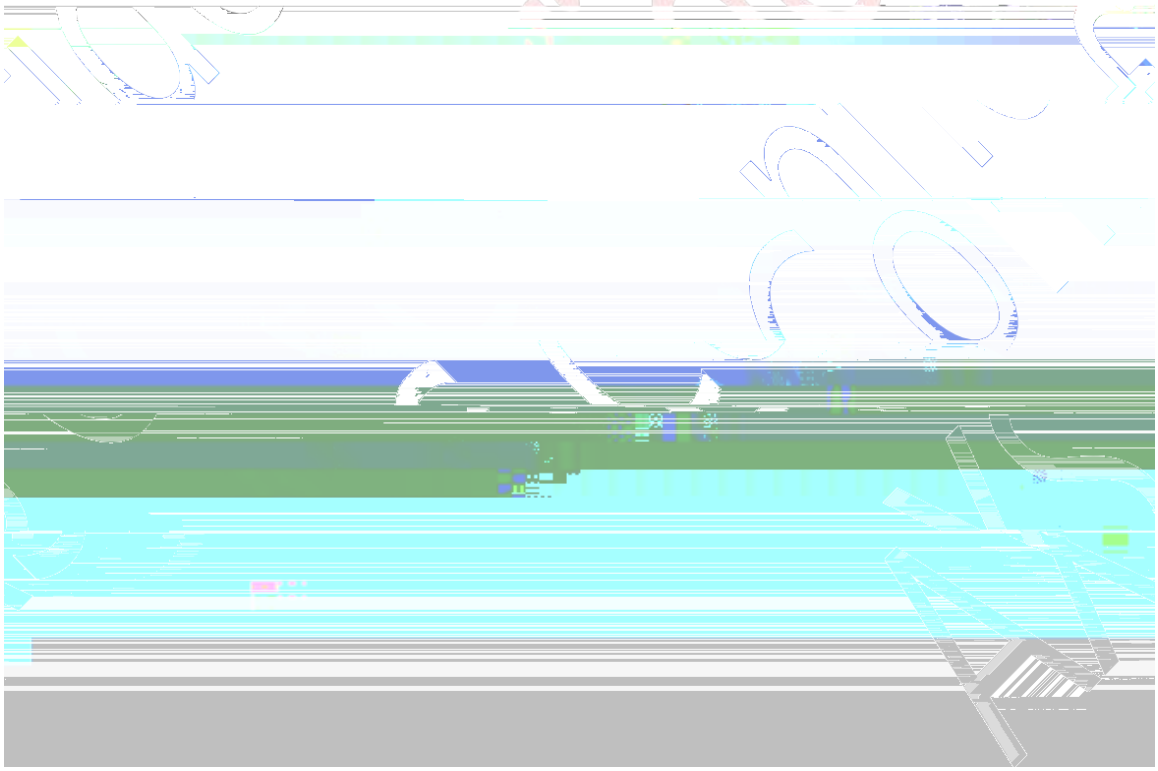
6. AC Electrical Characteristics

T_A = 25℃, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 4 Ω (unless otherwise noted)



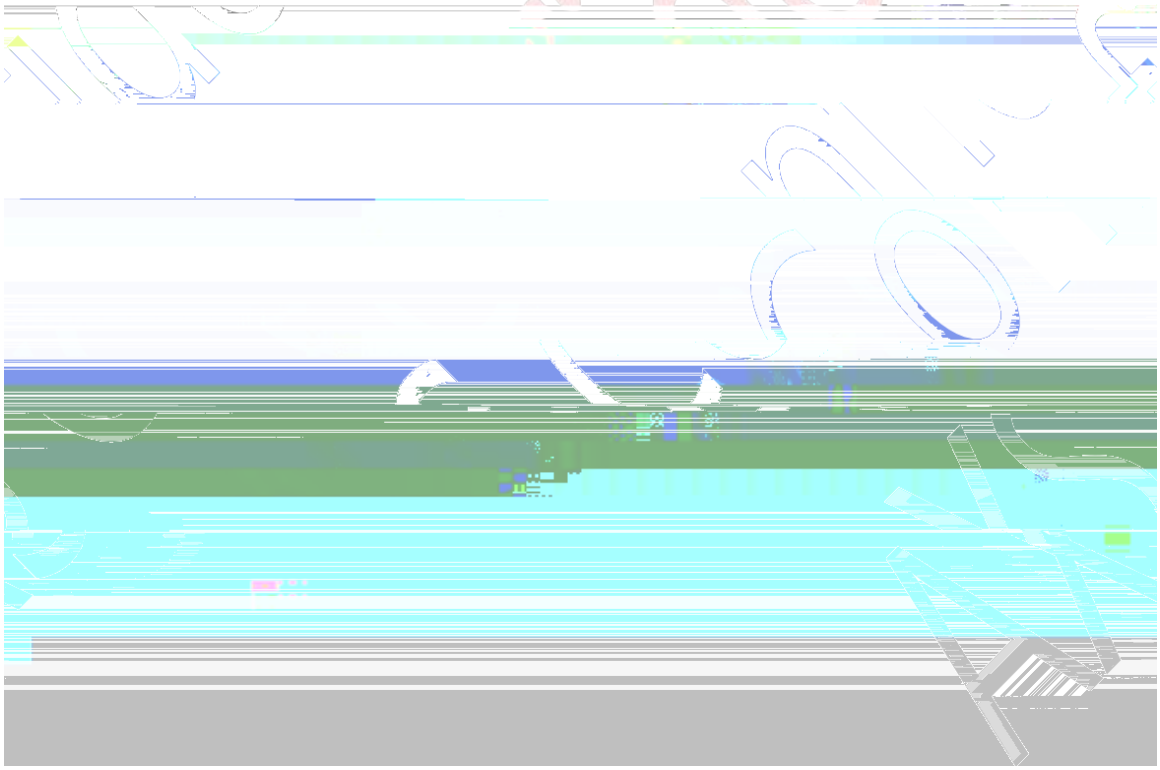
7. Typical Characteristics

f_S = 400kHz(unlessotherwisenoted)



Typical Characteristics (continued)

f_S = 400kHz(unlessotherwisenoted)



Detailed Description

1. Overview

The AXS2050 is a high efficiency Class-D audio power amplifier with AM interference suppression. The device operates from a single supply and can deliver 2x50W into 4Ω loads with 10% THD+N. The AM interference suppression function can be configured by the I²C interface to avoid the AM interference.

2. Functional Block Diagram

3. Feature Description

3.1 Gain Setting and Master and Slave

The gain of AXS2050 is set by the voltage applied to the GAIN/SLV pin. A voltage divider is used to apply one of eight voltages to the GAIN/SLV pin. Internal to the AXS2050 are nominal 300-kΩ resistors between the GAIN/SLV pin and the GVDD pin and between the GAIN/SLV pin and the GND pin. Table 1 lists the eight gain settings and the corresponding external resistor values.

Table 1. Gain and Master/Slave

MASTER / SLAVE MODE	GAIN	R1 (to GND)(1)	R2 (to GVDD)(1)	INPUT IMPEDANCE

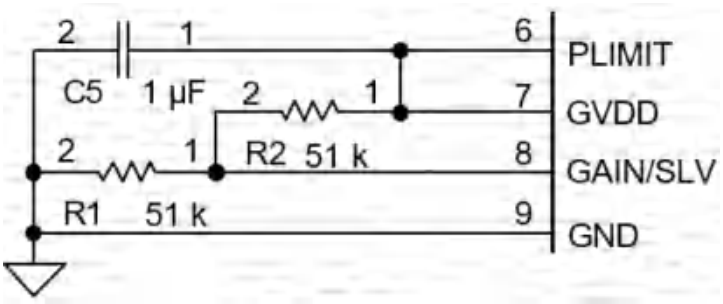


Table2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE	INPUT CAPACITANCE	HIGH-PASS FILTER
0 dB	6 k	5 nF	2 Hz
0 dB	3 k	3 nF	9 Hz
3 dB	1 k	6 nF	3 Hz
6 dB	7 k	0 nF	2 Hz

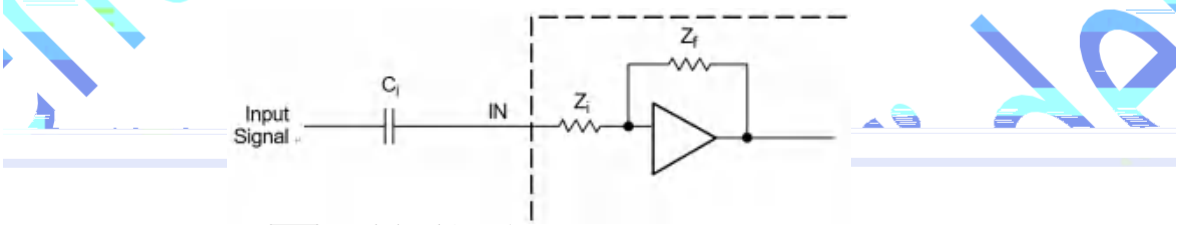
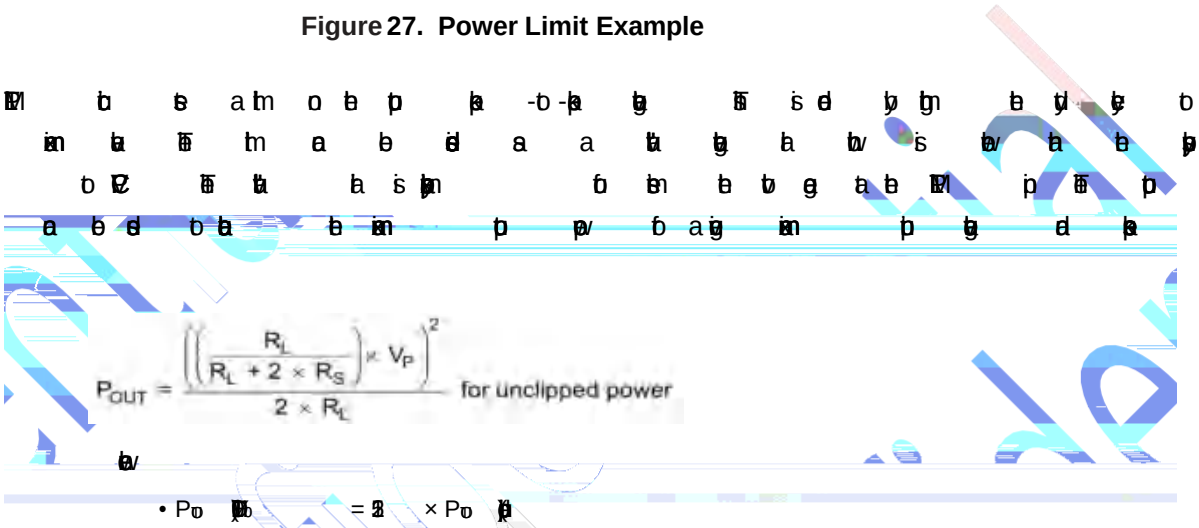


Figure 26. Input Impedance

3.3 Startup and Shutdown Operation

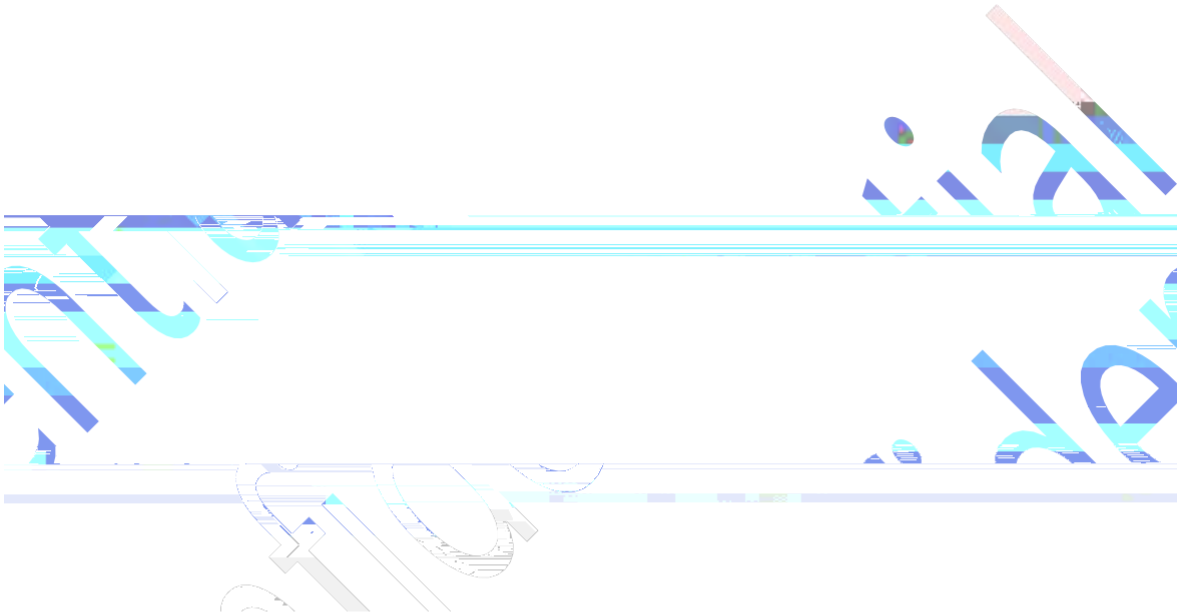
Figure 27. Power Limit Example



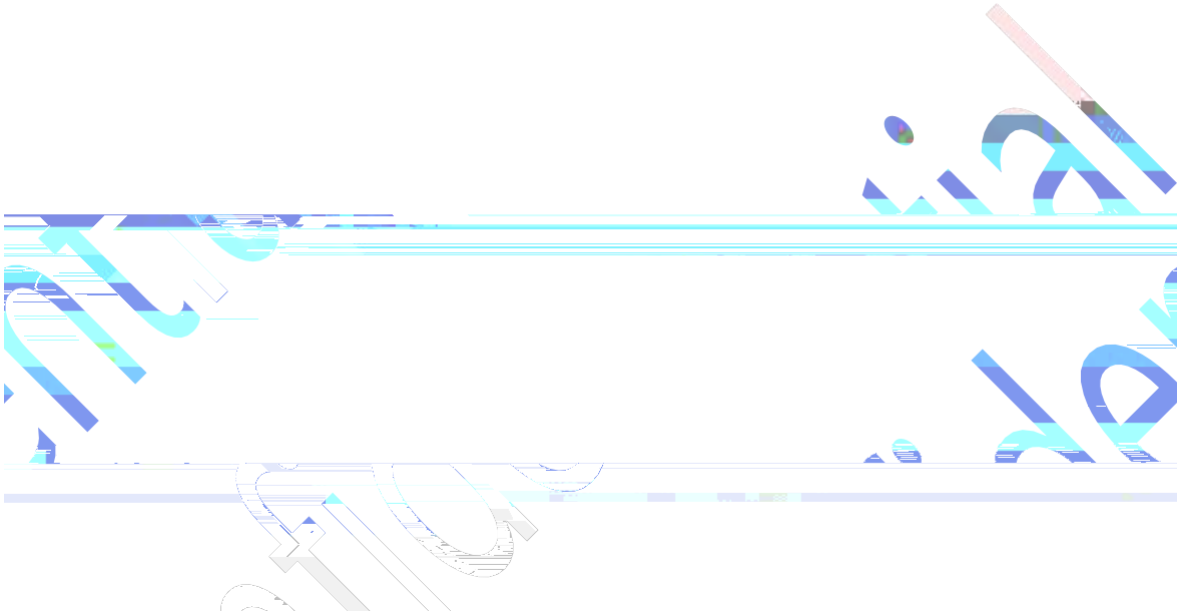
- Table 3. Power Limit Example

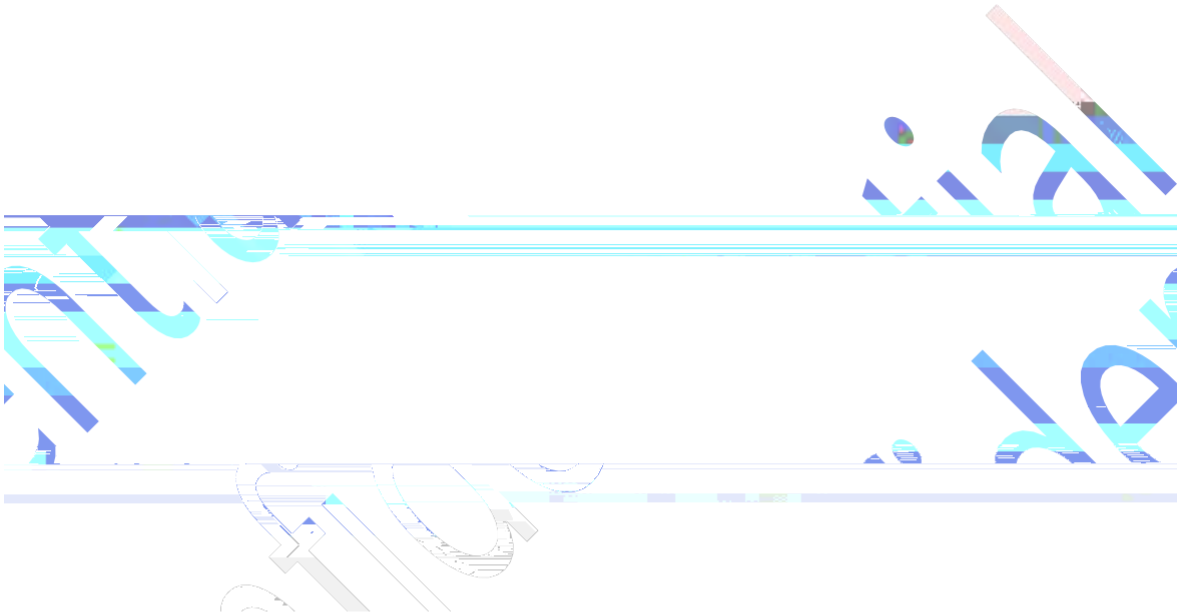
PVcc (V)	PLIMIT VOLTAGE (V)(1)	R to GND	R to GVDD	

3.9 DC Detect Protection



4. Device Modulation Scheme





7. When to Use an Output Filter for EMI Suppression

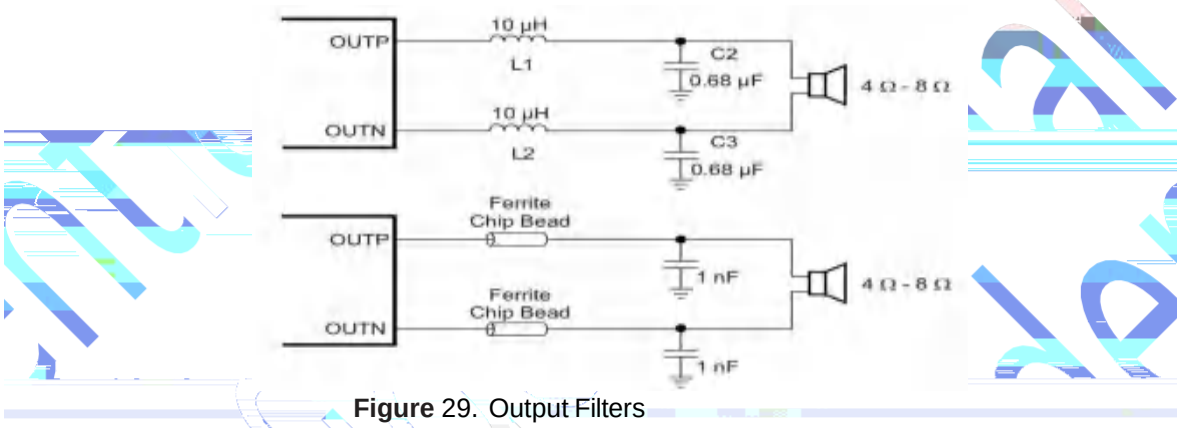


Figure 29. Output Filters

8. AM Avoidance EMI Reduction

Table 6. AM Frequencies

US	EUROPEAN	SWITCHING FREQUENCY (kHz)	AM2	AM1	AM0
AM FREQUENCY (kHz)	AM FREQUENCY (kHz)				
6 -2	6 -9	6	0	0	1
2 -1	9 -2	0 ǫ 0	0 0	1 0	0 0
1 -3	2 -3	6	0	0	1
3 -5	3 -8	0 ǫ 0	0 0	1 0	0 0
5 -0	8 -1	0 ǫ 0	0 0	1 0	0 1

9. Device Functional Modes

5 a b g in b a b 3

9.1 Mono PBTL Mode

h om B eh be id a id p b -W l pv G p f om B eh a a bv

- G N d N y b G w pa s e id is s in a om B eh g pv p
- G B d N g f e p pa an d D d D g f e g pa an
- y p g is d b N d N

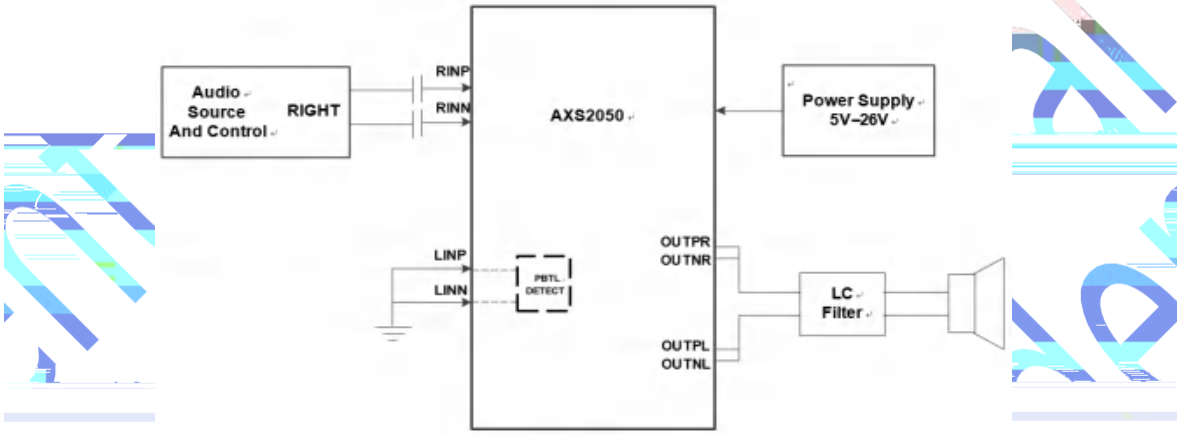


Figure 30. Mono PBTL Mode

9.2 Mono BTL

Mode (Single Channel Mode)

T A a e d in om B eh w g e d pv o

eh

Application Information

1. Typical Application

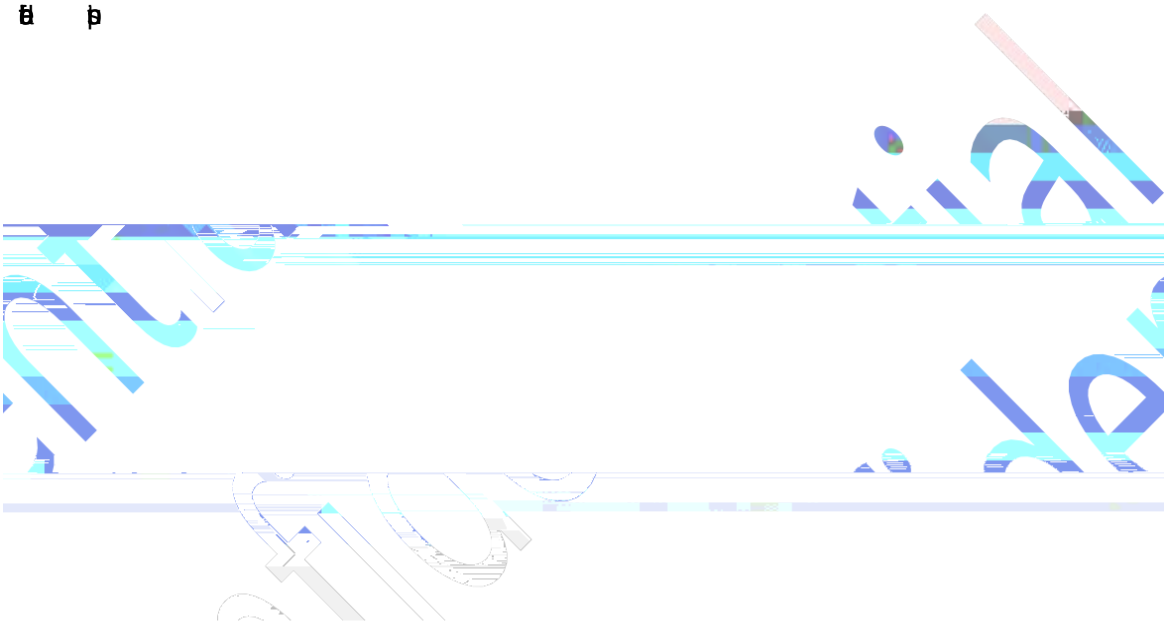


Figure 32. AXS2050 in a 2.1 Mode Application

2. Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
	5 V to

3. Detailed Design Procedure

- [illegible]

3.1 Select the PWM Frequency

[illegible]

3.2 Select the Amplifier Gain and Master/Slave Mode

[illegible]

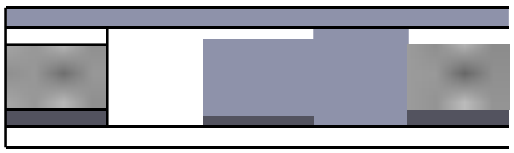
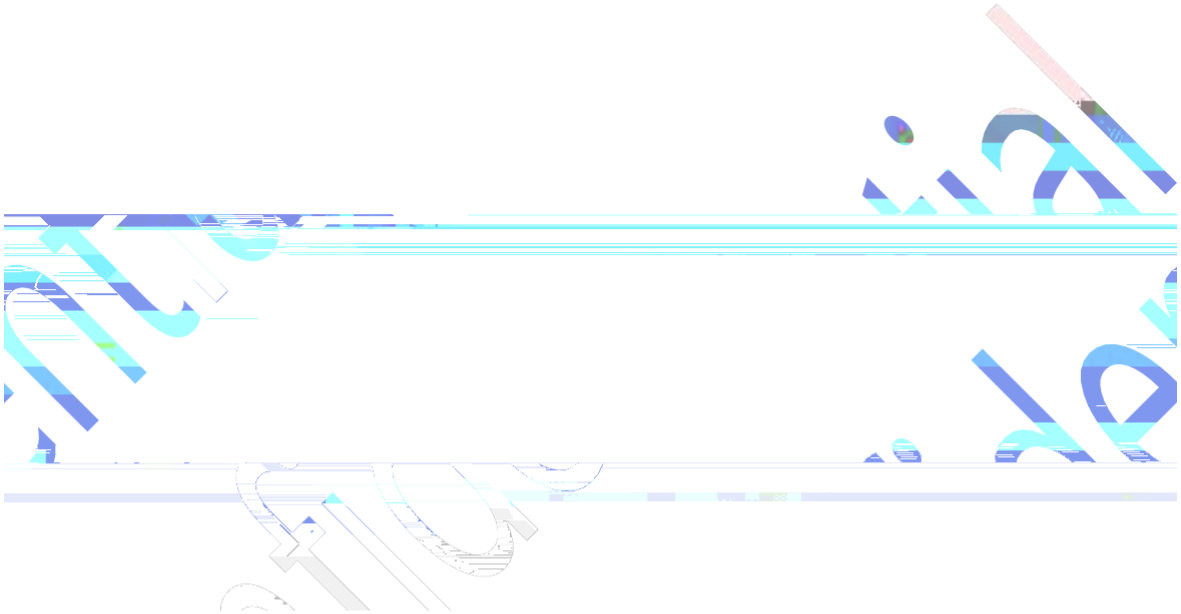
3.3 Select Input Capacitance

[illegible]

3.4 Select Decoupling Capacitors

[illegible]

3.5 Select Bootstrap Capacitors

[illegible]

6. Heat Sink Used on the EVM